SV6256P Datasheet

Low Power WiFi Dual Band 802.11 a/b/g/n SoC

General Description

The SV6256P is a low-power single chip device with the highest level of integration for internet of thing embedded systems. It is designed to support all mandatory IEEE 802.11b data rates of 1, 2, 5.5 and 11 Mbps, all 802.11g payload data rates of 6, 9, 12, 18, 24, 36, 48 and 54 Mbps, as well as 802.11n MCS0~MCS7, HT20/HT40, 800ns and 400ns guard interval.

It includes a dual band WLAN CMOS efficient power amplifier (PA) and an internal low noise amplifier (LNA). The Radio Frequency Front-end is single-ended bi-directional input and output.

The SV6256P has additional LDOs and DCDC buck convertor that could provide noise isolation for digital and analog supplies and excellent power efficient with minimum BOM cost.

While they both provide multiple peripheral interfaces including SPI_MASTER, UART_DATA, UART_DEBUG, I2C, I2S, etc.

The only external clock source needed for SV6256P based designs is a high speed crystal or oscillator. SV6256P support a variety of reference clocks which include 19.2, 20, 24, 25, 26, 38.4, 40 and 52 MHz. The USB application only support two reference clocks which are 25MHz and 40MHz.

SV6256P Features

- All CMOS IEEE 802.11 a/b/g/n single chip
- Single stream 802.11n provides highest throughput and superior RF performance for embedded system
- Advanced 1x1 802.11n features:
  - Full / Half Guard Interval
  - Frame Aggregation
  - Space Time Block Coding (STBC)
  - Greenfield mode
- Integrated WLAN CMOS efficient power amplifier with internal power detector and closed loop power calibration
- Package
  - QFN 48L, 6x6 mm, 0.4mm pitch

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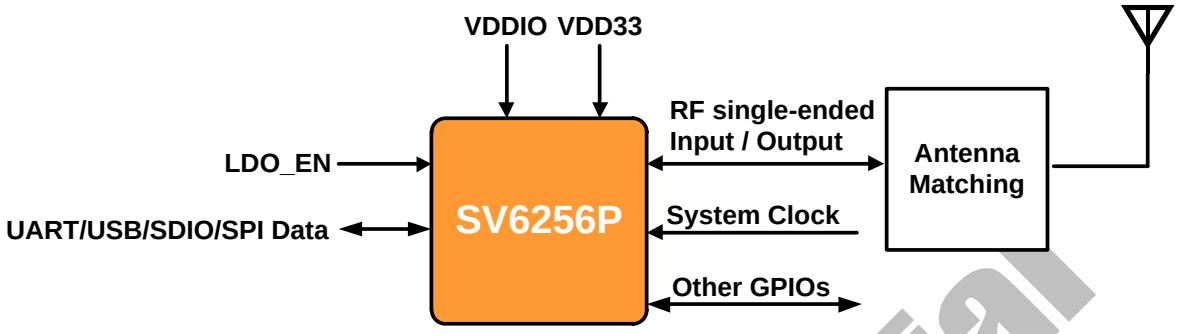

SV6256P System Block Diagram

Application SPI Data	Interface											XTAL	
	SPI Data	SDIO	USB	UART	I2C	SPI Master	PWM	ADC	I2S	Flash	PSRAM	19.2M~52M Hz	25M/40M Hz
SPI Data	1											v	
SDIO		1										v	
USB			1										v
IOT				2	1	1	5	4	1	1	1	v	

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Revision History

Version	Date	Description
1.0	2021/03/02	Initial release

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1 System Overview

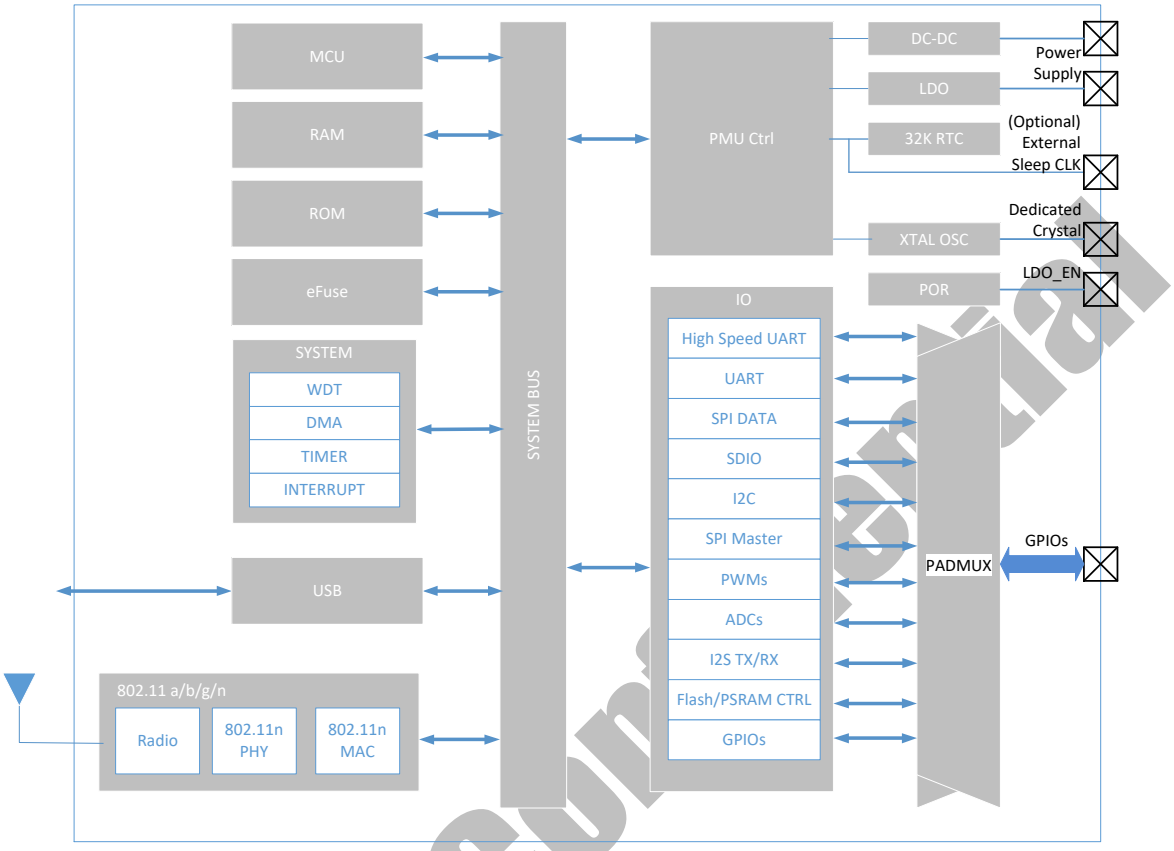

Figure 1: SV6256P Block Diagram

1.1 General Description

The SV6256P WLAN is designed to support IEEE 802.11 a/b/g/n single stream with the state of-the-art design techniques and process technology to achieve low power consumption and high throughput performance to address the requirement of mobile and handheld devices. The SV6256P WLAN low power function uses the innovative design techniques and the optimized architecture which best utilizes the advanced process technology to reduce active and idle power, and achieve extreme low power consumption at sleep state to extend the battery life. The SV6256P WLAN A-MPDU Tx function maximizes the throughput performance while achieving the best buffer utilization.

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1.2 MAC FEATURES

- 802.11 a/b/g/n/e/i/d
- 802.11n features
  - A-MPDU Tx & Rx
  - Support immediate Block-Ack
- AP/STA mode
  - Soft-AP
- Rate adaption mechanism
- WFA features
  - WEP/TKIP/WPA/WPA2
  - WMM/WMM PS

1.3 PHY FEATURES

- 802.11b, 11g, 11a, and 802.11n 1T1R
- Short Guard Interval
- Greenfield mode
- STBC in RX mode
- Enhanced and robust sensitivity for wider coverage range
- Supports calibration algorithm to handle no-idealities effects from CMOS RF block

1.4 SYSTEM

- Andes Technology N10 processor w/ ILM/DLM and I-cache
- 128K ROM and 192 KB SRAM for Instruction and data SRAM in total
- 8K retention SRAM
- Suspend/Wake-up manger controller
- Two channel DMA off load CPU loading.
- One Flash controller supports both Flash and PSRAM up to 64MB/64Mb with XIP
- One I2S TX/RX channel for 8~32bits/8~192KHz in master/slave mode.
- One SPI master
- One I2C
- One UART_Debug
- Four 10-bit ADC for IOT
- Five PWMs
- Four millisecond timers
- Four microsecond timers
- Two watchdog
- All pins can be multiplexed to GPIO by user scenario

1.5 HOST INTERFACE

- High Speed UART
  - Support RTSN/CTSN/RX/TX, 4 pins
  - Baud rate up to 4.8MHz
- UART
  - Support RX/TX, 2 pins
  - Baud rate up to 921600
- SPI Data
  - Provide proprietary/user CMD
- SDIO , SDIO 2.0 support both 1.8v and 3.3v in VIO

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- USB

1.6 System Clocking and Reset

The SV6256P has a system clocking block and reset which controls the clocks and power going to other internal modules. Its inputs consist of sleep requests from these modules and its outputs consist of clock enable and power signals which are used to gate the clocks going to internal modules. The system clocking and reset block also manages resets going to other modules within the device.

1.7 Design for Test

It also has features which enable testing of digital blocks via ATPG scan, memories via MBIST, analog components, and the radio.

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2 POWER SUPPLIES AND POWER MANAGEMENT

2.1 GENERAL DESCRIPTION AND PMU POWER CONNECTION

The power management unit (PMU) contains Low Dropout Regulators (LDOs), buck DC-DC converter and reference bandgap circuit.

The PMU integrated multi-LDOs and one buck converter. Those circuits are optimized for the given functions by balancing quiescent current, dropout voltage, line / load regulation, ripple rejection and output noise.

The input voltage of the buck converter is 3.3V. Its output voltage is 1.6V and feeds into the input power of the RF circuit and DLDO which has 1.2V output voltage for all digital circuits.

Figure 2 shows the typical power connection for SV6256P. DLDO and some RF circuits are powered by the buck converter output. The VDDIO is a power input which may be 3.3V from the host side. The connection structure is shown in the figure below.

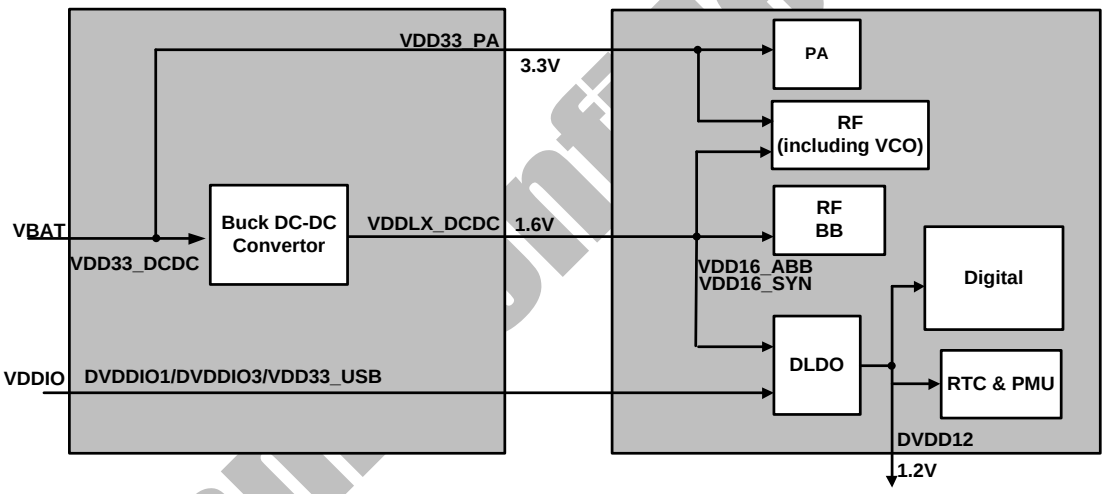

Figure 2 : SV6256P Power Connection

2.2 DLDO

The DLDO is integrated in the PMU to supply digital core. It converts voltage from 1.6V input to 1.2V output which suits the digital circuits. The input is typically connected to the buck's output.

2.3 BUCK CONVERTER

The regulator is a DC-DC step-down converter (buck converter) to source 300mA (max.) with 2.0V to 1.5V programmable output voltage based on the register setting. It supplies power for the RF circuit and DLDO.

2.4 POWER MANAGEMENT CONTROL

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There are three power modes that SV6256P operates when it is initialized: HOST_OFF, ACTIVE mode and SLEEP mode. There are two intermediate system transition modes: FW_DOWNLOAD and WARM_UP mode. The following are the brief introduction to each mode.

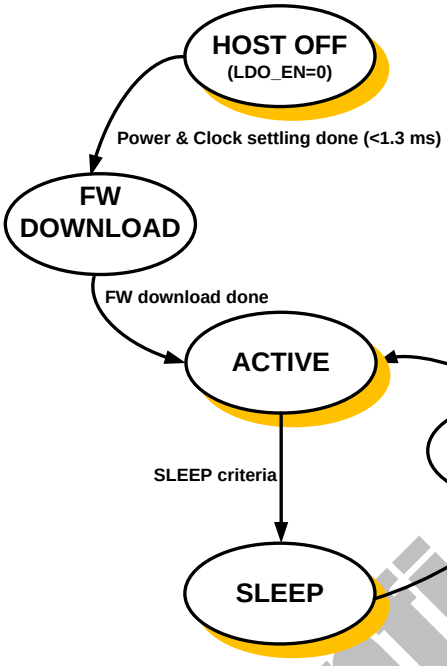

Figure 3: SV6256P Power State

Table 1: SV6256P Power State Description

State	Description
HOST OFF	When **LDO_EN** pin is de-asserted and logically low, the chip is brought to this state immediately.
	Sleep clock and internal power supply is disabled.
	After **LDO_EN** pin is asserted, the internal power and clock will be settled down within 1.3 ms.
FW DOWNLOAD	States for firmware download after power and clock is settled down.
SLEEP	The host controller can determine when to enter sleep to turn off most circuit in SV6256P. All the RF, DPLL circuits are turned off. In sleep mode, the system could be awakened after the sleep time is expired or by an external wake up signal from the host controller.
	All internal states are maintained and the Crystal oscillator is disabled.
WARM UP	The system transitions from SLEEP to ACTIVE. The crystal or oscillator is brought up and the PLL is enabled.
ACTIVE	The high speed clock is operational and sent to each block by the clock control register.
	The RF circuit is enabled to transmit or receive data, and the whole system is under normal operation.

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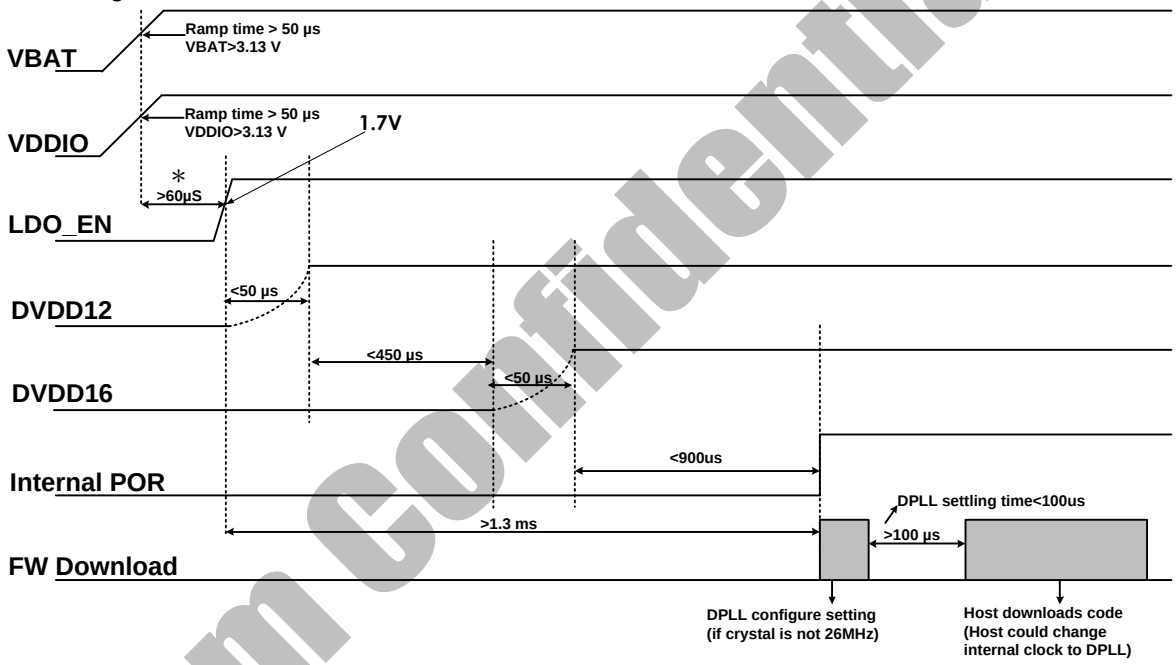
2.5 POWER-ON SEQUENCE

Figure 4 shows the power-on sequence of the SV6256P from power-up to firmware download, including the initial device power-on reset evoked by LDO_EN signal. The LDO_EN input level must be kept the same as VDDIO voltage level. After initial power-on, the LDO_EN signal can be held low to turn off the SV6256P or pulsed low to induce a subsequent reset. After LDO_EN is assert and host starts the power-on sequence of the SV6256P. From that point, the typical SV6256P power-on sequence is shown below:

1. Within 1.3 millisecond, the internal power-on reset (POR) will be done. And host could download firmware code of DPLL setting if the crystal is not default setting, 26MHz. The internal running clock is crystal frequency.
2. After 100us of DPLL settling time, host could set internal clock to full speed and finish all the downloading of firmware code.



Note: *

For IOT application, the timing between VDDIO and LDO_EN should be greater than [external flash VCC (min) to /CS Low+ 60us]. For example, if we use W25Q16JV as external flash, the timing between VDDIO and LDO_EN should be greater than (20us+60us).

Figure 4: Power-on sequence

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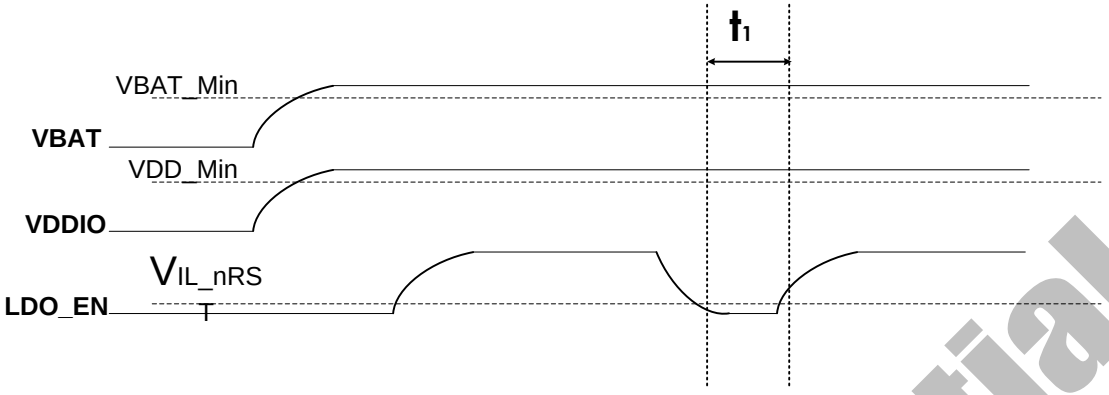

Figure 5 : Reset Timing

Table 2: Reset Timing Parameters

Parameters	Description	Min.	Unit
t_1	Duration of LDO_EN signal level < V_{IL}_nRST to reset the chip	30	us

2.6 RESET CONTROL

The SV6256P **LDO_EN** pin can be used to completely reset the entire chip. After this signal has been de-asserted, the SV6256P is in off mode waits for host communication. Until then, the MAC, BB, and SOC blocks are powered off and all modules are held in reset. Once the host has initiated communication, the SV6256P turns on its crystal and later on DPLL. After all clocks are stable and running, the resets to all blocks are automatically de-asserted.

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3 INTERFACE DESCRIPTION

3.1 SPI DATA TIMING WAVEFORM

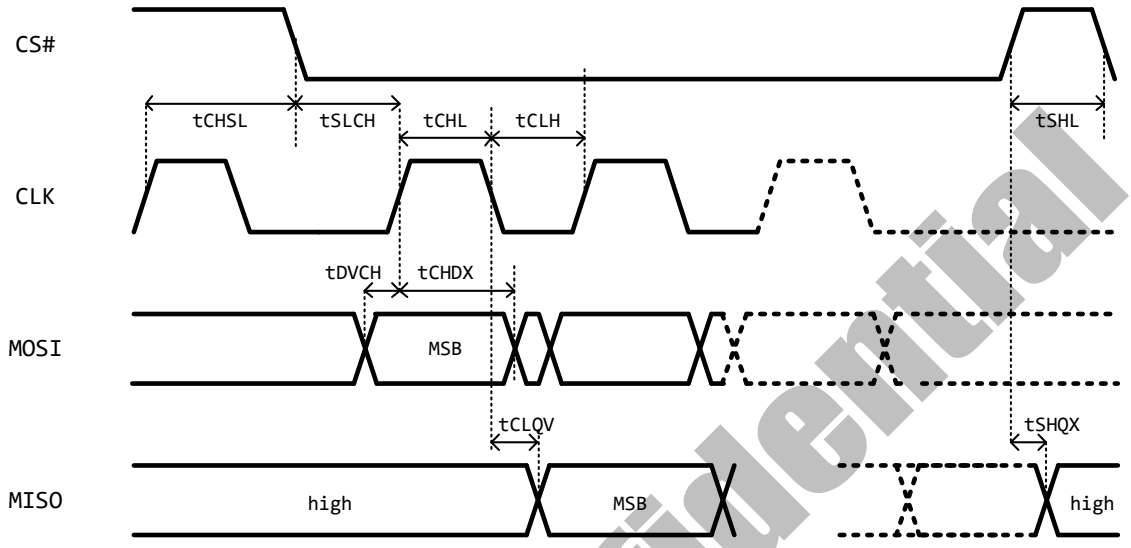

Figure 6: SPI Data TIMING WAVEFORM

Table 3: SPI Data Timing Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
tCHSL	CS# active hold time	10			ns
tSLCH	CS# active setup time	3			ns
tSHL	CS# inactive time	300			ns
tCHL	CLK high time	12.5			ns
tCLH	CLK low time	12.5			ns
tDVCH	Data in (MISO) setup time	3			ns
tCHDX	Data in (MISO) hold time	3			ns
tCLQV	Data output delay			6.5	ns
tSHQX	Data output disable time			6	ns

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3.2 SDIO TIMING WAVEFORM

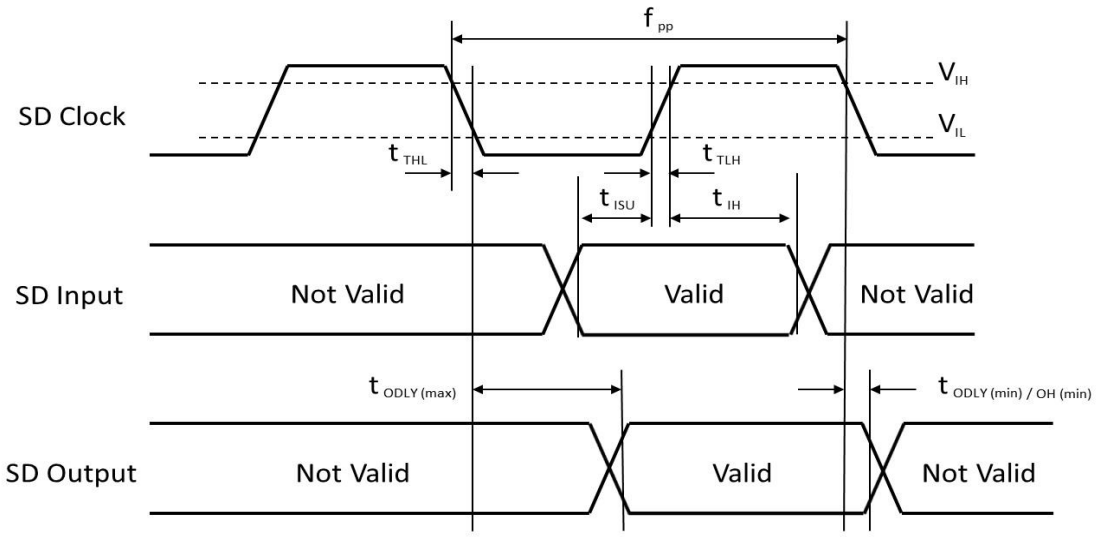

Figure 7: SDIO Timing Waveform

Table 4: SDIO version 2.0 Timing Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Clock CLK (All values are referred to min(V_{IH}) and max (V_{IL}).					
f_{pp}	Clock frequency Data Transfer Mode	0		50	MHz
t_{TLH}	Clock rise time			3	ns
t_{THL}	Clock fall time			3	ns
Inputs CMD, DAT (reference to CLK)					
t_{ISU}	Input set-up time	6			ns
t_{IH}	Input hold time	2			ns
Outputs CMD, DAT (reference to CLK)					
t_{ODLY}	Output Delay time during Data Transfer Mode			14	ns
t_{OH}	Output Hold time	2.5			Ns

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3.3 USB Timing Waveform

Table 5: USB High-Speed Source Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Driver characteristics						
tHSRLEW	Slew rate of rising edge	-	-	-	1600	V/usec
tHSFLEW	Slew rate of falling edge	-	-	-	1600	V/usec
Driver waveform	-	Specified by eye pattern template in USB2.0 spec.	-	-	-	-
Clock Timings						
THSRDRATE	High-speed data rate		479.76	-	480.24	Mbps
High-Speed Data Timings						
TJ	Data source jitter	Source and receiver jitter specified by the eye pattern template defined in USB2.0 spec.				
RXJT	Receiver jitter tolerance					

Table 6: USB Full-Speed Source Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Driver characteristics						
tFR	Rise time	CL = 50 pF 10% ~ 90% of |VOH – VOL|	4	-	20	ns
tHSFLEW	Fall time	CL = 50 pF 90% ~ 10% of |VOH – VOL|	4	-	20	ns
tFRMA	Differential rise/fall time matching (tFR/tFF)	Specified by eye pattern template in USB2.0 spec.	90	-	110	%
Clock Timings						
TFSTXDRATE	Full-speed TX data rate		11.994	-	12.006	Mbps
TFSRXDRATE	Full-speed RX data rate		11.97	-	12.03	Mbps
Full-Speed Data Timings						
TFDEOP	Source jitter for differential transition to SE0 transition	-	-2	-	5	ns
TJR1	Receiver jitter	To next transition	18.5	-	18.5	ns
TJR2	Receiver jitter	For paired transition	-9	-	9	ns
TFEOPT	Source SE0 interval of EOP	-	160	-	175	ns
TFEOPR	Receiver SE0 interval of EOP	-	82	-	-	ns
TFST	Width of SE0 interval during differential transition	-	-	-	14	ns

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Table 7: USB Low-Speed Source Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Driver characteristics						
tFR	Rise time	CL = 200 pF~ 600pF 10% ~ 90% of |VOH–VOL|	75	-	300	ns
tHSFLEW	Fall time	CL = 200pF ~ 600pF 90% ~ 10% of |VOH–VOL|	75	-	300	ns
tFRMA	Differential rise/fall time matching (tFR/tFF)	Specified by eye pattern template in USB2.0 spec.	80	-	125	%
Clock Timings						
TFSTXDRATE	Low-speed TX data rate		1.49925	-	1.50075	Mbps
TFSRXDRATE	Low-speed RX data rate		1.49925	-	1.50075	Mbps
Full-Speed Data Timings						
TFDEOP	Source jitter for differential transition to SE0 transition	-	-40	-	100	ns
TJR1	Receiver jitter	To next transition	-75	-	75	ns
TJR2	Receiver jitter	For paired transition	-45	-	45	ns
TFEOPT	Source SE0 interval of EOP	-	1.25	-	1.5	ns
TFEOPR	Receiver SE0 interval of EOP	-	670	-	-	ns
TFST	Width of SE0 interval during differential transition	-	-	-	210	ns

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4 DC CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings in Table 8 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 8: Absolute Maximum Ratings

Symbol (domain)	Description	Max Rating	Unit
VDD16	VDD input for analog 1.6V	-0.3 to 3.6	V
VDD33_SX	VDD input for external components I/O control	-0.3 to 3.6	V
VDD33_RF	VDD input for external components I/O control	-0.3 to 3.6	V
DVDDIO1	VDD input for I/O	-0.3 to 3.6	V
DVDDIO3	VDD input for I/O	-0.3 to 3.6	V
VDD33_USB	VDD input for I/O	-0.3 to 3.6	V
DVDD12	VDD output for internal digital circuit	-0.3 to 1.32	V
VDD16_DCDC	VDD input for digital circuit's LDO	-0.3 to 3.6	V
VDD33_DCDC	VDD input for DCDC	-0.3 to 3.6	V

4.2 ENVIRONMENTAL RATINGS

The environmental ratings are shown in Table 9: Environmental Ratings

Table 9: Environmental Ratings

	Part Number	Value	Units
Operating Temperature(T_A)	SV6256P	-40 to +85	°C

4.2.1 Storage Condition

The calculated shelf life in sealed bag is 12 months if stored between 0°C and 40°C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

a) Mounted within 168 hours of factory conditions < 30 **°C** /60%RH
b) Storage humidity needs to maintained at <10% RH
c) Baking is necessary if customer exposes the component to air over 168 hours, baking condition: 125°C / 8 hours

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4.3 THERMAL CHARACTERISTICS

Thermal characteristics without external heat sink in still air condition

Table 10: The thermal characteristics of the SV6256P

Symbol	Description	Typ.	Unit
T_J	Maximum Junction Temperature (Plastic Package)	125	°C
θ_{JA}	Thermal Resistance θ_{JA} (°C /W) for JEDEC 4L system PCB	37.8	°C/W
θ_{JC}	Thermal Resistance θ_{JC} (°C /W) for JEDEC 4L system PCB	TBD	°C/W
Ψ_{Jt}	Thermal Characterization parameter Ψ_{Jt} (°C /W) for JEDEC 4L system PCB	4.13	°C/W
	Maximum Lead Temperature (Soldering 10s)	260	°C

Notes: * JEDEC 51-7 system FR4 PCB size: 3” x 4.5” (76.2 x 114.3 mm)
* Thermal characteristics without external heat sink in still air condition

4.4 ELECTROSTATIC DISCHARGE SPECIFICATIONS

This is an ESD sensitive product. Observe precaution and handle with care. Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices.

Table 11: ESD Specifications

Pin Type	Test Condition	ESD Rating	Unit
Human Body Mode (HBM)	refers to MIL-STD-883G Method 3015.7	Pass ±2.5	KV
Charged Device Model(CDM)	JEDEC –500 +500 V specification JESD22-C101, all pins	Pass ±500	V

4.5 POWER-ON HOURS(POH)

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Table 12: Power-On Hours

OPERATION CONDITION	Part Number	Power-On Hours(POH)(hours)
T_A up to 85°C [a]	SV6256P	87600

a. The TX duty cycle (power amplifier ON time) is assumed to be 10% of the device POH. Of the remaining 90% of the time, the device can be in any other state.

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4.6 Recommended Operating Conditions and DC Characteristics

Table 13: Recommended Operating Conditions and DC Characteristics

Domain(Symbol)	Description	Min.	Typ.	Max.	Unit
VDD16	VDD input for analog 1.6V		1.6		V
VDD33_SX	VDD input for external components I/O control	3.13	3.3	3.46	V
VDD33_RF	VDD input for external components I/O control	3.13	3.3	3.46	V
DVDDIO1	VDD input for GPIO pins	3.13	3.3	3.46	V
DVDDIO3	VDD input for GPIO pins (same level as DVDDIO1)	3.13	3.3	3.46	V
VDD33_USB	VDD input for HSDP/HSDM	3.13	3.3	3.46	V
	VDD input for GPIO pins	1.71	3.3	3.46	
DVDD12	VDD output for internal digital circuit		1.2		V
VDD16_DCDC	VDD input for digital circuit's LDO		1.6		V
VDD33_DCDC	VDD input for DCDC	3.13	3.3	3.46	V
(V_{IL})	Input Low voltage when VDDIO=3.3V	-0.3		0.8	V
	Input Low voltage when VDDIO=1.8V	-0.3		0.6	V
(V_{IH})	Input High voltage when VDDIO=3.3V	2		3.6	V
	Input High voltage when VDDIO=1.8V	1.2		3.6	V
(V_{T+})	Schmitt trigger low to high threshold voltage when VDDIO=3.3V	1.6	1.74	1.89	V
	Schmitt trigger low to high threshold voltage when VDDIO=1.8V	1.03	1.07	1.15	V
(V_{T-})	Schmitt trigger high to low threshold voltage when VDDIO=3.3V	1.27	1.4	1.56	V
	Schmitt trigger high to low threshold voltage when VDDIO=1.8V	0.67	0.7	0.72	V
(V_{OL})	Output low voltage when VDDIO=3.3V			0.4	V
	Output low voltage when VDDIO=1.8V			0.45	V
(V_{OH})	Output high voltage when VDDIO=3.3V	2.4			V
	Output high voltage when VDDIO=1.8V	1.3			V

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Domain(Symbol)	Description	Min.	Typ.	Max.	Unit
(R_{PD})	Input weakly pull-down resistance when VDDIO=3.3V. All GPIO pins have internal weakly pull- down option except that GPIO_5 has internal weakly pull-up option				KΩ
(R_{PU})	Input weakly pull-high resistance when VDDIO=3.3V. All GPIO pins have internal weakly pull- down option except that GPIO_5 has internal weakly pull-up option				KΩ
(I_{OL})	Low level output current @ V_{OL}(max), 8mA setting	11.9	17.7	23.4	mA
	Low level output current @ V_{OL}(max), 12mA setting	15.8	23.5	31.1	mA
(I_{OH})	High level output current @ V_{OH}(min), 8mA setting	17.2	34.1	58.8	mA
	High level output current @ V_{OH}(min), 12mA setting	23.9	47.2	81.5	mA

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5 FREQUENCY REFERENCES

5.1 CRYSTAL OSCILLATOR SPECIFICATIONS

Table 14: Crystal Oscillator Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range	–	Between 19.2MHz~52MHz			
Crystal load Capacitance	–	–	10		pF
ESR	–	–	–	70	Ω
Frequency tolerance Initial and over temperature	–	-20ppm	–	20ppm	ppm

5.2 EXTERNAL CLOCK-REQUIREMENTS AND PERFORMANCE

Table 15: External Clock-Requirements and Performance

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range	–	Between 19.2MHz~52MHz			
OSCIN Input Voltage	AC-couple analog signal	400	–	1500	mV_{PP}
Frequency tolerance Initial and over temperature	–	-20ppm	–	20ppm	ppm
Duty Cycle	26MHz clock	40	50	60	%
Phase Noise (802.11a/b/g)	26MHz clock at 1KHz offset	–	–	–119	dBc/Hz
	26MHz clock at 10KHz offset	–	–	–129	dBc/Hz
	26MHz clock at 100KHz offset	–	–	–134	dBc/Hz
	26MHz clock at 1MHz offset	–	–	–139	dBc/Hz
Phase Noise (802.11n 2.4/5GHz)	26MHz clock at 1KHz offset	–	–	–125	dBc/Hz
	26MHz clock at 10KHz offset	–	–	–135	dBc/Hz
	26MHz clock at 100KHz offset	–	–	–140	dBc/Hz
	26MHz clock at 1MHz offset	–	–	–145	dBc/Hz

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6 Electrical Specifications

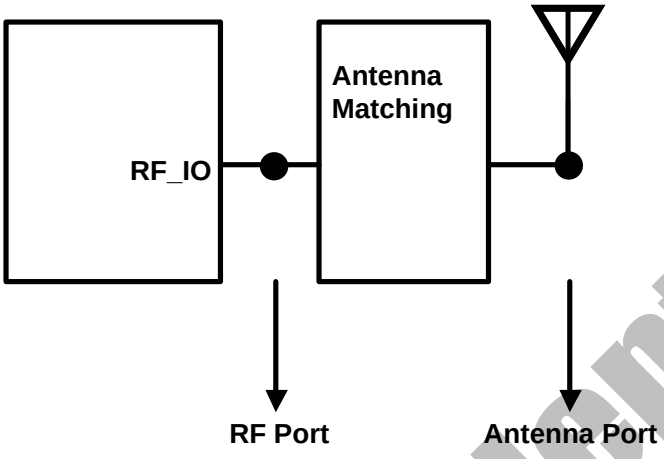

Figure 8: RF Front-End Reference Topology for RF Performance

Note: All specifications are measured at the RF Port unless otherwise specified.

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6.1 WLAN RF PERFORMANCE SPECIFICATIONS

Table 16: 2.4G WLAN RF Performance Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range		2412	-	2484	MHz
Rx Sensitivity (CCK)	CCK, 1 Mbps		-95.5		dBm
	CCK, 2 Mbps		-93.5		dBm
	CCK, 5.5 Mbps		-91.0		dBm
	CCK, 11 Mbps		-88.0		dBm
Rx Sensitivity (OFDM)	OFDM, 6 Mbps		-91.5		dBm
	OFDM, 9 Mbps		-90.0		dBm
	OFDM, 12 Mbps		-88.0		dBm
	OFDM, 18 Mbps		-86.0		dBm
	OFDM, 24 Mbps		-82.5		dBm
	OFDM, 36 Mbps		-79.5		dBm
	OFDM, 48 Mbps		-74.5		dBm
	OFDM, 54 Mbps		-73.5		dBm
Rx Sensitivity (HT20) Greenfield 800nS GI Non-STBC	HT20, MCS0		-91.0		dBm
	HT20, MCS1		-88.0		dBm
	HT20, MCS2		-86.0		dBm
	HT20, MCS3		-81.5		dBm
	HT20, MCS4		-79.0		dBm
	HT20, MCS5		-74.5		dBm
	HT20, MCS6		-73.5		dBm
	HT20, MCS7		-72.5		dBm
Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
RX Adjacent Channel Rejection (CCK)	CCK, 1 Mbps (30 MHz offset)		41		dB
	CCK, 11 Mbps (25 MHz offset)		41		dB
RX Adjacent Channel Rejection (OFDM)	OFDM, 6 Mbps (25 MHz offset)		39		dB
	OFDM, 54 Mbps (25 MHz offset)		23		dB
RX Adjacent Channel Rejection (HT20)	HT20, MCS0 (25 MHz offset)		38		dB
	HT20, MCS7 (25 MHz offset)		21		dB
TX Output Power (with PADPD)	CCK, 1-11 Mbps		19		dBm
	OFDM, 54 Mbps		16		dBm
	HT20, MCS7		15		dBm

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Table 17: 5G WLAN RF Performance Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range		5180	-	5850	MHz
Rx Sensitivity (OFDM)	OFDM, 6 Mbps		-91.0		dBm
	OFDM, 9 Mbps		-89.5		dBm
	OFDM, 12 Mbps		-88.0		dBm
	OFDM, 18 Mbps		-86.0		dBm
	OFDM, 24 Mbps		-82.5		dBm
	OFDM, 36 Mbps		-79.5		dBm
	OFDM, 48 Mbps		-74.5		dBm
	OFDM, 54 Mbps		-73.5		dBm
Rx Sensitivity Greenfield 800nS GI Non-STBC	HT20, MCS0		-90.0		dBm
	HT20, MCS1		-87.5		dBm
	HT20, MCS2		-85.5		dBm
	HT20, MCS3		-81.5		dBm
	HT20, MCS4		-79.0		dBm
	HT20, MCS5		-74.5		dBm
	HT20, MCS6		-73.0		dBm
	HT20, MCS7		-72.0		dBm
	HT40, MCS0		-87.0		dBm
	HT40, MCS7		-68.5		dBm
Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
RX Adjacent Channel Rejection (OFDM)	OFDM, 6 Mbps (20 MHz offset)		28		dB
	OFDM, 54 Mbps (20 MHz offset)		19		dB
RX Adjacent Channel Rejection (HT20)	HT20, MCS0 (20 MHz offset)		27		dB
	HT20, MCS7 (20 MHz offset)		6		dB
TX Output Power (with PADPD)	OFDM, 54 Mbps		13.5		dBm
	HT20, MCS7		13		dBm
	HT40, MCS7		13		dBm

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7 System Power Consumption

Table 18: Power Consumption at DCDC mode (DCDC buck convertor is enable)

WLAN Operational Modes	Typ.[d]	Unit
OFF[a]	2	uA
Rx, CCK, 1 Mbps	68	mA
Rx, OFDM, 54 Mbps	68	mA
Rx, HT20, MCS7	68	mA
Rx, HT40, MCS7	75	mA
Rx, 5.18G HT20, MCS7	88	mA
Rx, 5.805G HT20, MCS7	88	mA
Rx, 5.18 G HT40, MCS7	97	mA
Rx, 5.805G HT40, MCS7	97	mA
Tx, CCK, 1 Mbps	307	mA
Tx, OFDM, 54 Mbps@15dBm	256	mA
Tx, HT20, MCS7@15dBm	260	mA
Tx, HT40, MCS7@15dBm	260	mA
Tx, 5.18 G HT20, MCS7	310	mA
Tx, 5.805G HT20, MCS7	293	mA

Table 19: Power Consumption at LDO mode (DCDC buck convertor is disable)

WLAN Operational Modes	Typ.[d]	Unit
OFF[a]	2	uA
Rx, CCK, 1 Mbps	113	mA
Rx, OFDM, 54 Mbps	113	mA
Rx, HT20, MCS7	113	mA
Rx, HT40, MCS7	124	mA
Rx, 5.18G HT20, MCS7	133	mA
Rx, 5.805G HT20, MCS7	133	mA
Rx, 5.18 G HT40, MCS7	142	mA
Rx, 5.805G HT40, MCS7	142	mA
Tx, CCK, 1 Mbps@18dBm	328	mA
Tx, OFDM, 54 Mbps@15dBm	280	mA
Tx, HT20, MCS7@15dBm	283	mA
Tx, HT40, MCS7@15dBm	285	mA
Tx, 5.18 G HT20, MCS7	356	mA
Tx, 5.805G HT20, MCS7	335	mA

a. OFF mode test condition: VBAT=3.3V, VIO=3.3V, LDO_EN=0V.
b. Intra-beacon Sleep when MCU is turn on.
It is used in the applications that require the CPU to be working.
c. Intra-beacon Sleep when MCU is turn off.
d. Conditions: VBAT at 3.3v, VDDIO at 3.3V, 25°C.

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8 Pin Descriptions

This section contains a listing of the signal descriptions (see Figure 9 for the SV6256P QFN package pin-out)

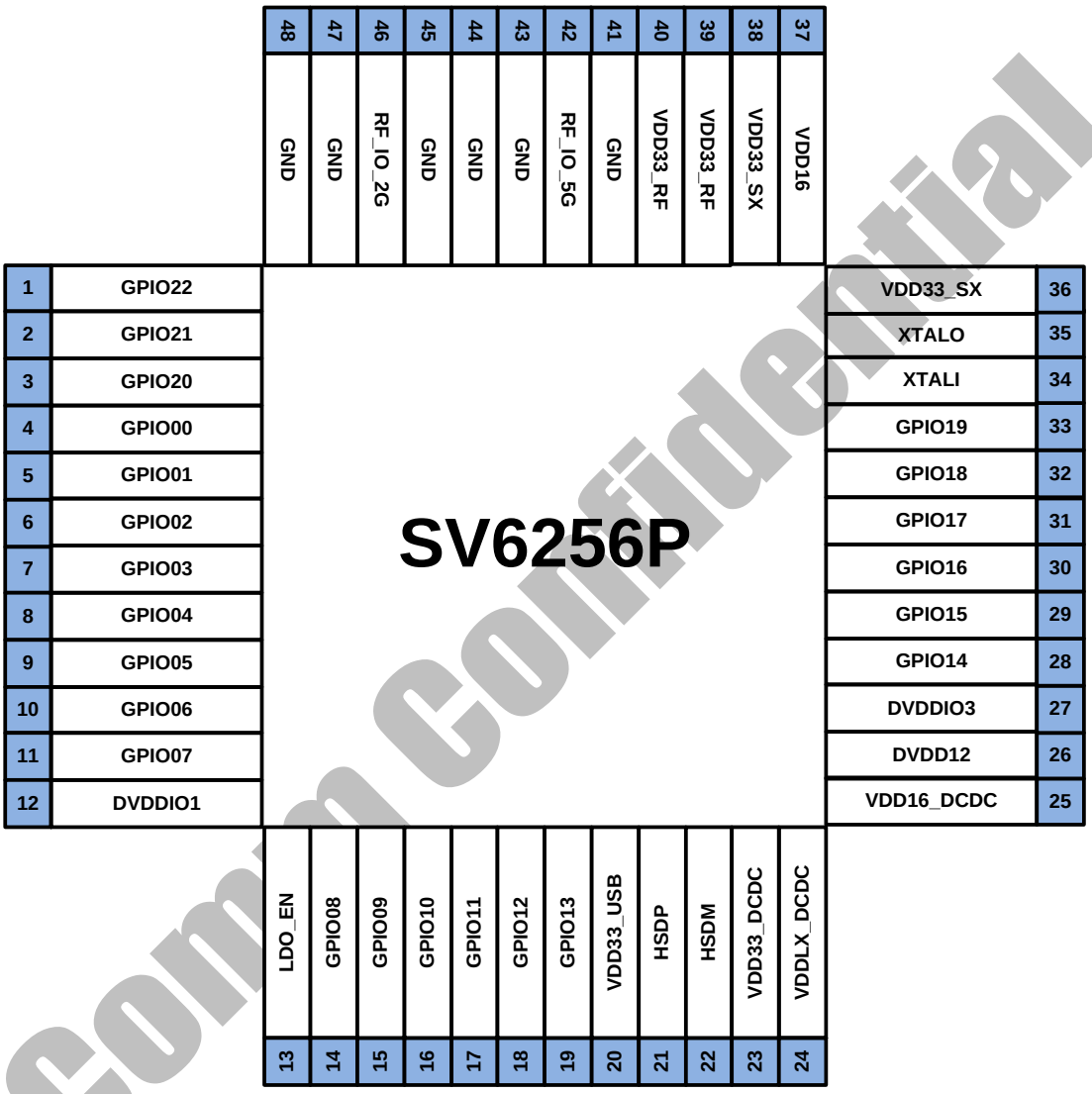

Figure 9: SV6256P QFN Pin Assignment (top view)

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Table 20: SV6256P Package Pin-out

No.	Name	Description	Type
1	GPIO22	General Purpose I/O Pins	I/O
2	GPIO21	General Purpose I/O Pins	I/O
3	GPIO20	Strapping Purpose I/O Pins	I/O
4	GPIO00	General Purpose I/O Pins	I/O
5	GPIO01	General Purpose I/O Pins	I/O
6	GPIO02	General Purpose I/O Pins	I/O
7	GPIO03	General Purpose I/O Pins	I/O
8	GPIO04	General Purpose I/O Pins	I/O
9	GPIO05	General Purpose I/O Pins	I/O
10	GPIO06	General Purpose I/O Pins	I/O
11	GPIO07	Strapping Purpose I/O Pins	I/O
12	DVDDIO1	VIO input for GPIO00~07/GPIO20~22	Power
13	LDO_EN	Reset signal to power down IC	Input
14	GPIO08	General Purpose I/O Pins	I/O
15	GPIO09	General Purpose I/O Pins	I/O
16	GPIO10	General Purpose I/O Pins	I/O
17	GPIO11	General Purpose I/O Pins	I/O
18	GPIO12	General Purpose I/O Pins	I/O
19	GPIO13	General Purpose I/O Pins	I/O
20	VDD33_USB	VIO input for GPIO08~13/HSDP/HSDM	Power
21	HSDP	HSDP	I/O
22	HSDM	HSDM	I/O
23	VDD33_DCDC	analog 3.3V input for DCDC	Power
24	VDDLX_DCDC	DCDC buck regulator: output to inductor	Power
25	VDD16_DCDC	DCDC 1.6V	Power
26	DVDD12	Digital 1.2V input	Power
27	DVDDIO3	VIO input for GPIO14~19	Power
28	GPIO14	Strapping Purpose I/O Pins	I/O
29	GPIO15	Strapping Purpose I/O Pins	I/O
30	GPIO16	General Purpose I/O Pins	I/O
31	GPIO17	General Purpose I/O Pins	I/O
32	GPIO18	General Purpose I/O Pins	I/O
33	GPIO19	General Purpose I/O Pins	I/O
34	XTALI	Input of crystal clock reference	Input
35	XTALO	Output of crystal clock reference	output
36	VDD33_SX	analog 3.3V input	Power
37	VDD16	analog 1.6V input	Power
38	VDD33_SX	analog 3.3V input	Power
39	VDD33_RF	analog 3.3V input	Power
40	VDD33_RF	analog 3.3V input	Power
41	GND	Ground	GND
42	RF_IO_5G	5 GHz RF input & output port	RF I/O
43	GND	Ground	GND

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No.	Name	Description	Type
44	GND	Ground	GND
45	GND	Ground	GND
46	RF_IO_2G	2.4 GHz RF input & output port	RF I/O
47	NC	NC Pin	NC
48	NC	NC Pin	NC

8.1 INTERFACE SELECTION

SV6256P has bootstrap pins to select interface which including debug interface, host I/O. There are GPIO07, GPIO14, GPIO15 and GPIO20 (see Table 21 for detail). The bootstrap pin of GPIO07 decides switching the debug interface out to GPIOs (see Table 22 for detail). The bootstrap pins of GPIO14 and GPIO15 decode switch the host IO out to GPIOs (see /Table 24/Table 25/Table 26). The bootstrap pin of GPIO20 decides switching 25MHz or 40MHz clock when using USB interface (see Table 21 for detail).

Table 21: The strapping truth table

strapping truth table		
	Interface mode	**Description**
GPIO[07]		
0	AICE debug	for ICE debug interface
1	NC	NC (default)
GPIO[15], GPIO[14]		
00	SPIFL-E	SPI flash w/I in-place execution (default)
01	SPIDATA	SPI data mode
10	SDIO	SDIO mode
11	USB	USB mode
GPIO[20]		
0	USB_XO25M	for USB 25MHz clock (default)
1	USB_XO40M	for USB 40MHz clock

Table 22: The strapping pin of GPIO07

GPIO07		Low			High			
Pin No.	Name	I/O	PULL	I/O Function SPIFL-E/SPIDATA/SDIO/USB	I/O	PULL	I/O Function SPIFL-E	I/O Function SPIDATA/SDIO/USB
4	**GPIO00**	I/O	F	TMSC	I/O	F	GPIO00	NC
5	**GPIO01**	I	F	TCKC	I	F	GPIO01	NC
6	**GPIO02**	I	PU	nSRST	I	PU	GPIO02	NC
7	**GPIO03**	I	F	UART0_RXD	I	F	GPIO03	NC
8	**GPIO04**	O	F	UART0_TXD	O	F	NC	NC

Table 23: The strapping pin of GPIO14/15 for Flash/PSRAM interface

GPIO15/14		2'b00		
Pin No.	**Name**	**I/O**	**PULL**	**I/O Function**
9	**GPIO05**	O	F	UART1_RTS
10	**GPIO06**	I	F	UART1_RXD
11	**GPIO07**	O	PU	UART1_TXD
14	**GPIO08**	I/O	F	GPIO08
15	**GPIO09**	I	F	UART1_CTS
16	**GPIO10**	I/O	F	GPIO10
17	**GPIO11**	I/O	F	GPIO11
18	**GPIO12**	I/O	F	GPIO12
19	**GPIO13**	O	PU	SPI_PSRAM_CSN
28	**GPIO14**	I/O	PD	SPI_flash_IO0_DI (MOSI)
29	**GPIO15**	O	PD	SPI_flash_CLK
30	**GPIO16**	I/O	PU	SPI_flash_IO3_HD
31	**GPIO17**	O	PU	SPI_flash_CSN
32	**GPIO18**	I/O	PD	SPI_flash_IO1_DO (MISO)
33	**GPIO19**	I/O	PU	SPI_flash_IO2_WP
3	**GPIO20**	I/O	F	GPIO20
2	**GPIO21**	I	F	GPIO21
1	**GPIO22**	I/O	F	GPIO22

Table 24: The strapping pin of GPIO14/15 for SPI DATA slave interface

GPIO15/14		2'b01		
Pin No.	**Name**	**I/O**	**PULL**	**I/O Function**
9	**GPIO05**	O	F	NC
10	**GPIO06**	I	F	NC
11	**GPIO07**	O	PU	Strapping
14	**GPIO08**	O	F	SPI0_S_INT
15	**GPIO09**	I	F	NC
16	**GPIO10**	I	F	SPI0_S_MOSI
17	**GPIO11**	I	F	SPI0_S_CLK
18	**GPIO12**	O	F	SPI0_S_MISO
19	**GPIO13**	I	F	SPI0_S_CSN
28	**GPIO14**	I/O	F	Strapping
29	**GPIO15**	I/O	F	Strapping
30	**GPIO16**	I/O	F	NC
31	**GPIO17**	I/O	F	NC
32	**GPIO18**	I/O	F	NC
33	**GPIO19**	I/O	F	NC
3	**GPIO20**	O	F	GPIO20(WIFI_WAKE_HOST)
2	**GPIO21**	I	F	GPIO21(HOST_WAKE_WIFI)
1	**GPIO22**	O	F	NC

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Table 25: The strapping pin of GPIO14/15 for SDIO interface

GPIO15/14		2'b10		
Pin No.	Name	I/O	PULL	I/O Function
9	GPIO05	O	F	NC
10	GPIO06	I	F	NC
11	GPIO07	O	PU	Strapping
14	GPIO08	I/O	F	SD_D2
15	GPIO09	I	F	SD_D3
16	GPIO10	I/O	F	SD_CMD
17	GPIO11	I/O	F	SD_CLK
18	GPIO12	I/O	F	SD_D0
19	GPIO13	O	F	SD_D1
28	GPIO14	I/O	F	Strapping
29	GPIO15	O	F	Strapping
30	GPIO16	I/O	F	NC
31	GPIO17	O	F	NC
32	GPIO18	I/O	F	NC
33	GPIO19	I/O	F	NC
3	GPIO20	I/O	F	GPIO20(WIFI_WAKE_HOST)
2	GPIO21	I	F	GPIO21(HOST_WAKE_WIFI)
1	GPIO22	I/O	F	NC

Table 26: The strapping pin of GPIO14/15 for USB slave interface

GPIO15/14		2'b11		
Pin No.	Name	I/O	PULL	I/O Function
9	GPIO05	O	F	NC
10	GPIO06	I	F	NC
11	GPIO07	O	PU	Strapping
14	GPIO08	O	F	NC
15	GPIO09	I	F	NC
16	GPIO10	I	F	NC
17	GPIO11	I	F	NC
18	GPIO12	O	F	NC
19	GPIO13	I	F	NC
28	GPIO14	I/O	F	Strapping
29	GPIO15	I/O	F	Strapping
30	GPIO16	I/O	F	NC
31	GPIO17	I/O	F	NC
32	GPIO18	I/O	F	NC
33	GPIO19	I/O	F	NC
3	GPIO20	O	F	GPIO20(WIFI_WAKE_HOST)
2	GPIO21	I	F	GPIO21(HOST_WAKE_WIFI)
1	GPIO22	O	F	NC

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8.2 User Define I/O Function Selection

After bootstrap, the IOT application also provides a pad multiplex switching from the bootstrap function to selected I/O function by register signals. There is a condition to leave bootstrap function. That is switching to GPIO first then switching to select I/O function. The Table 27 shows the all I/O functions for each PAD.

Table 27: The PAD multiplex for each PAD for IOT application

Pin No.	Pin Name	Alternate Functions		
4	GPIO00	I/O	F	GPIO[00]
		O	F	PWM0
5	GPIO01	I/O	F	GPIO[01]
		O	F	PWM1
6	GPIO02	I/O	F	GPIO[02]
		O	F	PWM2
7	GPIO03	I/O	F	GPIO[03]
		O	F	PWM3
		I	F	UART0_RXD
8	GPIO04	I/O	F	GPIO[04]
		O	F	PWM4
		O	F	UART0_TXD
9	GPIO05	I/O	F	GPIO[05]
		O	F	UART1_RTS
		I/O	F	I2S_BCLK
10	GPIO06	I/O	F	GPIO[06]
		I	F	UART1_RXD
		I	F	I2S_DI
11	GPIO07	I/O	F	GPIO[07]
		O	PU	UART1_TXD
		O	F	I2S_DO
14	GPIO08	I/O	F	GPIO[08]
		I/O	F	I2S_BCLK
		O	PD	SPI_M_CLK
15	GPIO09	I/O	F	GPIO[09]
		I	F	UART1_CTS
		I/O	F	I2S_LRCLK
16	GPIO10	I/O	F	GPIO[10]
		I	F	I2S_DI
		I	PU	SPI_M_MISO
		I/O	PU	I2C_SDA
17	GPIO11	I/O	F	GPIO[11]
18	GPIO12	I/O	F	GPIO[12]
		O	F	I2S_DO
		O	PU	SPI_M_MOSI
		O	PU	I2C_SCL

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Pin No.	Pin Name	Alternate Functions		
19	GPIO13	I/O	F	GPIO[13]
		I/O	F	I2S_LRCLK
		O	PU	SPI_M_CS
		O	PU	SPI_PSRAM_CSN
28	GPIO14	I/O	F	GPIO[14]
		I/O	PD	SPI_flash_IO0_DI
29	GPIO15	I/O	F	GPIO[15]
		O	PD	SPI_flash_CLK
30	GPIO16	I/O	F	GPIO[16]
		I/O	PU	SPI_flash_IO3_HD
31	GPIO17	I/O	F	GPIO[17]
		O	PU	SPI_flash_CSN
32	GPIO18	I/O	F	GPIO[18]
		I/O	PD	SPI_flash_IO1_DO
33	GPIO19	I/O	F	GPIO[19]
		I/O	PU	SPI_flash_IO2_WP
3	GPIO20	I/O	F	GPIO[20]
		O	F	I2S_MCLK
2	GPIO21	I/O	F	GPIO[21]
		O	PU	I2C_SCL
		O	F	UART0_TXD
1	GPIO22	I/O	F	GPIO[22]
		I/O	PU	I2C_SDA
		I	F	UART0_RXD

*If using SDIO/SPI DATA/USB application, IO pin function is fixed and defined by driver.

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8.3 IOT ADC

SV6256P IOT application provides an ADC named IOT_ADC for sensing external voltage. It is an inverse binary thermal code design, the more the voltage, the less the data read.

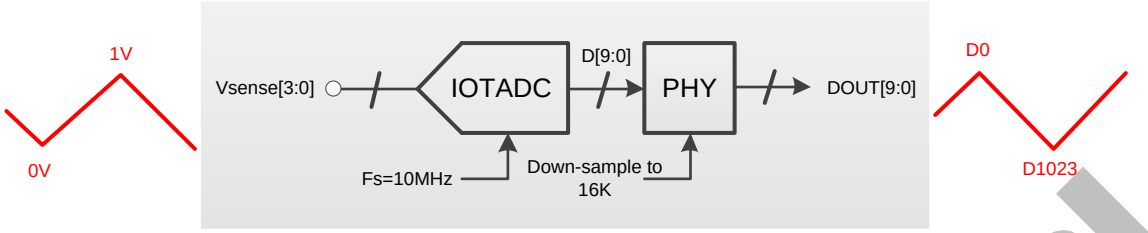

Figure 10: ADC Block diagram

Table 28: IOT ADC Pin Location

Pin No.	Pin Name	IOT ADC inputs
1	GPIO22	Vsense[0]
2	GPIO21	Vsense[1]
3	GPIO20	Vsense[2]
4	GPIO00	Vsense[3]

Table 29: IOT ADC Specifications

Parameter	Description	Condition/Notes	Min	Typ.	Max	Unit
Nbits	Number of bits			10		Bits
INL	Integral nonlinearity	Histogram method over full scale		±4		LSB
DNL	Differential nonlinearity	Histogram method over full scale		±2		LSB
Input Range			0		1	V
Input impedance				100K		Ohms
FCLK	Clock rate	Successive approximation input clock rate		10		MHz
Input capacitance				2		pF
Number of channels				4		
Fsample	Sampling rate of each ADC			16/8		KSPS
F_input_max	Maximum input signal frequency			7.2/3.6		kHZ
I_active	Active supply current	Average for ADC during conversion		1		mA
I_PD	Power-down supply current for core supply	Disable ADC		1		uA
Absolute offset error				±40		mV
Gain error				±2.5		%

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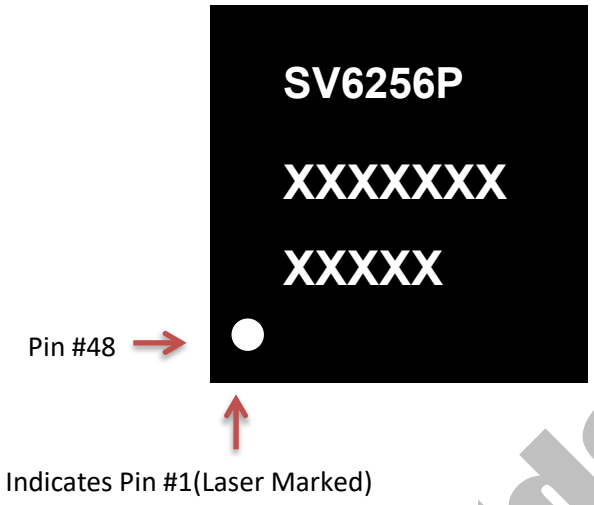
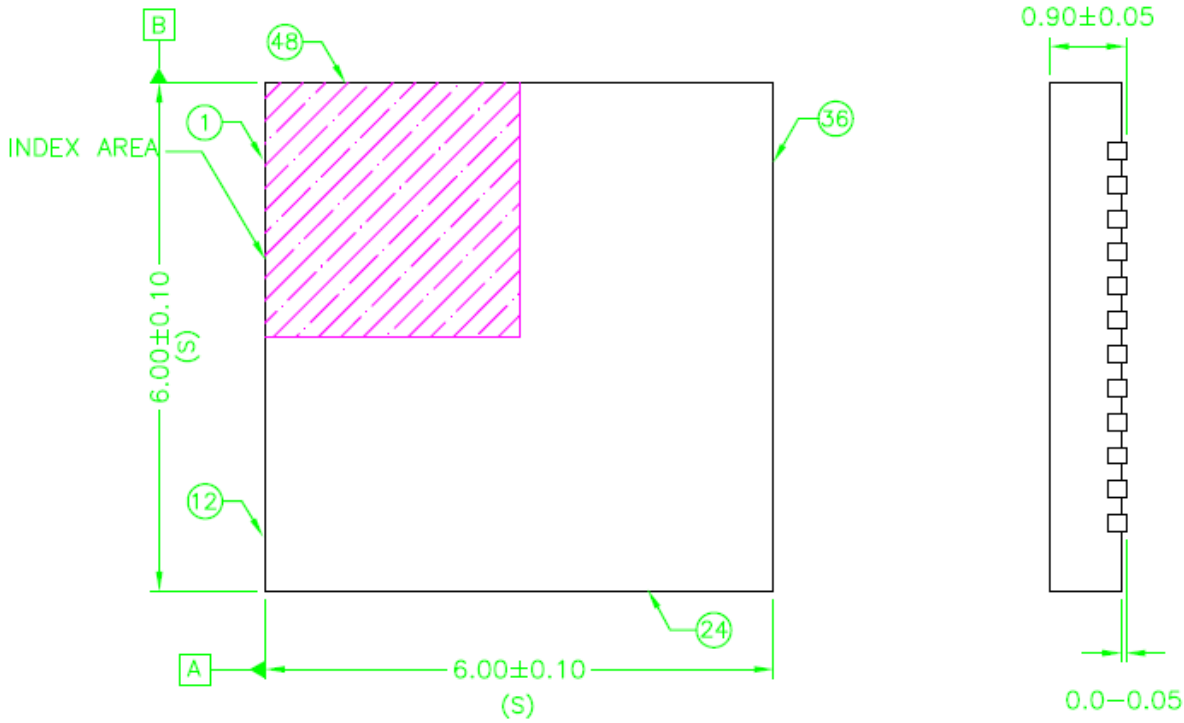
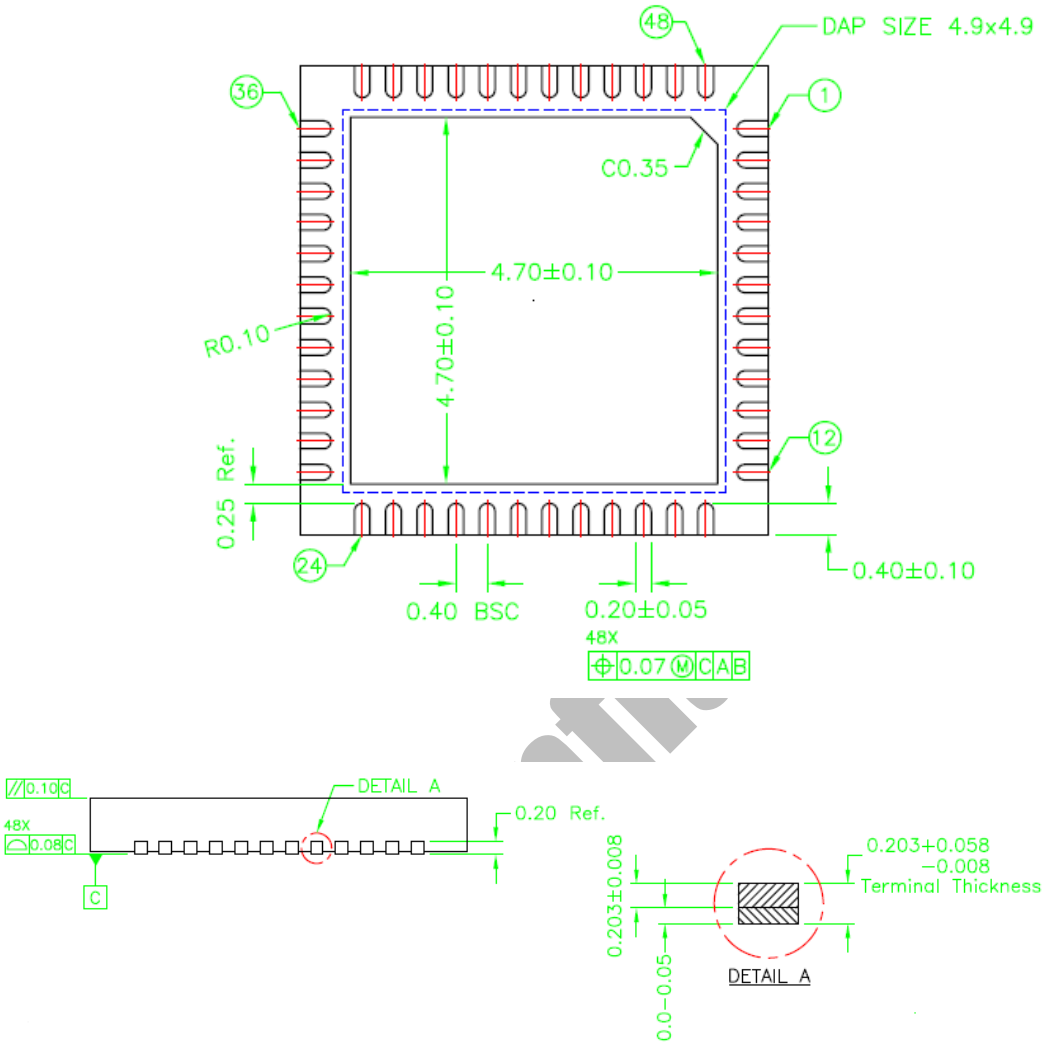
9 PACKAGE INFORMATION

6 x 6 mm (body size), 0.4mm pitch QFN-48

Marking format (top view)







NOTE :

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC. (S)
5. L/F STOCK# FR9012 (PPF)

Figure 11: QFN 6 x 6 mm Package Dimensions

10 Part Number

The table below provides the ordering information of the SV6256P.

Table 30: SV6256P Part Number

Part Number	Band	Operating Temp(°C)	Package
SV6256P	Dual Band	-40 to +85	QFN 6x6

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